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**APPLICATION
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MEMORY TESTING

Background of the Invention

1. Technical Field

The present invention relates to memory testing, and more specifically, to a memory chip
5 that facilitates memory testing.

2. Related Art

Testing of a memory array in a conventional memory chip using a tester involves running
a BIST (Built-In-Self-Test) circuit inside the memory chip through multiple testing passes. For
the first testing pass, the tester initializes the BIST and the BIST performs a predetermined
10 sequence of cycles. A cycle may be a write cycle, a read cycle, or a setup cycle. During a write
cycle, the BIST writes a test pattern (e.g., all 1s) into a location of the memory array. During a
read cycle, the BIST causes the content of a location of the memory array to be read and
compared with the expected data. If there is a mismatch, a fail signal is generated to the tester.
During a setup cycle, the BIST may do some setup without writing or reading the memory array.

15 As an example of the testing of the memory array of the conventional memory chip,
assume that during the first testing pass, the BIST sequentially and without pause runs from cycle
1d ("d" stands for decimal) to cycle 3000d, in which cycles 1d-2000d are setup and write cycles,
and cycles 2001d-3000d are read cycles. Assume further that at cycle 2200d, the read data is not
the same as the expected data. As a result, a fail signal is sent to the tester which records the
20 cycle number of the failing cycle (which is 2200d). Assume further that at cycle 2400d, the read

data is not the same as the expected data. As a result, a fail signal is sent to the tester which records the cycle number of the failing cycle (which is 2400d).

As a result, the tester has to run the BIST two more testing passes (the second and third testing passes) to collect fail data corresponding to the two failing cycles 2200d and 2400d.

5 More specifically, for the second testing pass, the tester initializes the BIST and the BIST performs the same predetermined sequence of cycles as in the first testing pass except that the BIST stops at cycle 2200d. Then, the read data is collected from the memory chip by scanning out the entire memory chip.

10 Then, for the third pass, the tester again initializes the BIST and the BIST performs the same predetermined sequence of cycles as in the first testing pass except that the BIST stops at cycle 2400d. Then, the read data is collected from the memory chip by scanning out the entire memory chip.

In general, if during the first testing pass, the tester records N failing cycles, the tester has to cause the BIST to run N more passes. It is always desirable to reduce the number of testing
15 passes the BIST needs to run.

Therefore, a design of a novel memory chip is needed that requires fewer BIST testing passes to test the memory chip than in prior art. A method is also needed for testing the novel memory chip.

Summary of the Invention

The present invention provides a structure comprising a BIST (Built-In-Self-Test) circuit; and a first memory circuit electrically coupled to the BIST circuit, wherein the BIST circuit is configured to perform a first test pass for the first memory circuit to collect the cycle numbers of failing cycles for the first memory circuit in response to the first memory circuit being selected for testing, and wherein, during a second test pass for the first memory circuit performed by the BIST after the first test pass for the first memory circuit, the BIST circuit is configured to collect the contents of the locations in the first memory circuit associated with the failing cycles for the first memory circuit.

The present invention also provides a method for testing a structure, the method comprising the steps of (a) providing in the structure a BIST (Built-In-Self-Test) circuit and a first memory circuit electrically coupled to the BIST circuit; (b) using the BIST circuit to perform a first test pass for the first memory circuit to collect the cycle numbers of failing cycles for the first memory circuit in response to the first memory circuit being selected for testing; and (c) after performing the first test pass for the first memory circuit, using the BIST circuit to perform a second test pass for the first memory circuit to collect the contents of the locations in the first memory circuit associated with the failing cycles for the first memory circuit.

The present invention also provides a method for testing a memory chip, the method comprising the steps of (a) providing in the memory chip a RAM (Random Access Memory) and a BIST (Built-In-Self-Test) circuit; (b) providing a RAM select register in the BIST circuit; (c)

scanning in a select value into the RAM select register so as to select the RAM for testing; (d) using the BIST circuit to test the RAM for a first test pass to collect the cycle numbers of failing cycles in response to the RAM being selected for testing; and (e) after testing the RAM for the first test pass, using the BIST circuit to test the RAM for a second test pass, wherein the second test pass comprises the same sequence of cycles as the first test pass, and wherein during the second test pass, the BIST circuit pauses at each failing cycle so that the contents of the locations of the RAM associated with the failing cycles can be extracted out of the memory chip.

The present invention provides structures for a memory chip that requires fewer BIST testing passes to test the memory chip than in prior art.

The present invention also provides methods for such a memory chip.

Brief Description of the Drawings

FIG. 1 illustrates a structure comprising a tester and a memory chip, in accordance with embodiments of the present invention.

FIG. 2 illustrates the flow chart of a method for operating the structure of FIG. 1.

Detailed Description of the Invention

FIG. 1 illustrates a structure 100 comprising a tester 110 and a memory chip 120, in accordance with embodiments of the present invention. Illustratively, the memory chip 120 comprises a BIST (Built-In-Self-Test) 130, RAM (Random Access Memory) circuits 140.1 and 140.2, and a chip multiplexer 150.

The BIST 130 comprises illustratively a finite state machine 131, a BIST control generator 132, a BIST address generator 133, a BIST data generator 134, a BIST state register 135, a RAM select register 136, and a BIST multiplexer 137.

The RAM 140.1 comprises illustratively a memory array 142.1, a data-out register 144.1, a comparator 146.1, and a mode multiplexer 148.1. Similarly, the RAM 140.2 comprises illustratively a memory array 142.2, a data-out register 144.2, a comparator 146.2, and a mode multiplexer 148.2.

In one embodiment, the BIST 130 can perform a predetermined sequence of cycles including write, read, and setup cycles. During a write cycle, assuming that the RAM 140.1 is being selected for testing, the BIST 130 writes a test pattern into a location of the memory array 142.1. More specifically, during the write cycle, the BIST control generator 132 generates control signals to the memory array 142.1 via connection 932. The control signals indicate to the memory array 142.1 that it is being written.

The BIST address generator 133 generates the address of that write location to the memory array 142.1 via connection 933. The BIST data generator 134 generates a test pattern (e.g., all 0s) to the memory array 142.1 via connection 934. As a result, the test pattern is written to the location of the memory array 142.1.

5 During a read cycle, assuming that the RAM 140.1 is being selected for testing, the BIST 130 reads out the content of a location of the memory array 142.1 which content is then compared with the expected data so as to detect a fail. More specifically, during the read cycle, the BIST control generator 132 generates control signals to the memory array 142.1 via connection 932. The control signals indicate to the memory array 142.1 that it is being read.

10 The BIST address generator 133 generates the address of that read location to the memory array 142.1 via connection 933. In response, the memory array 142.1 outputs the content of the read location to the data-out register 144.1 and then to the comparator 146.1 via connections 947.1. The BIST data generator 134 generates the expected pattern/data to the comparator 146.1 via connections 934 and 946.1. The comparator 146.1 compares the read data (on connection
15 947.1) and the expected data (on connection 946.1). If the two values are not equal, the comparator 146.1 pulls a Pass/Fail signal high on the connection 948.1. In response, the connections 949.1 and 950.1 are also pulled high (explained later). As a result, the connection 950 is also pulled high (explained later) indicating to the tester 110 that the current cycle is a failing cycle.

During a setup cycle, the BIST 130 performs setup within itself without reading from or writing to any RAM 140.1 or 140.2.

FIG. 2 illustrates the flow chart of a method 200 for operating the structure of FIG. 1.

With reference to both FIGS. 1 and 2, the operation of the structure 100, the connections between the components of the structure 100, and the method 200 will become clear during the discussion of the following example.

In this example, initially, in step 210 of the method 200, a scan-in of the entire memory chip 120 is performed so that the RAM select register 136 contains 0b ("b" indicates binary) so as to select the RAM 140.1 for testing. Scan-initialization of other circuits (not shown) causes the chip mux 150 to electrically couple the connections 949.1 and 950.1 (coming from RAM 140.1) to the connection 950 (leading to the tester 110). Multiple BISTs 130 may exist on the chip, and the other chip circuits (not shown) will cause the chip multiplexer to select one of the chip's SRAMs, whereas the BIST multiplexer 137 is used to select one of the SRAMs which share a given BIST.

The RAM select register 136 containing 0b causes the BIST multiplexer 137 to electrically couple the connections 937.1 and 949.1 (coming from RAM 140.1) to the connection 937 (leading to the BIST state register 135). As a result, the RAM 140.1 is selected and ready for testing.

Also in step 210, the tester 110 pulls low a control signal Diag_Shift which is coupled to the BIST state register 135 and the data-out registers 144.1 and 144.2 so that the memory chip 120 is in pass/fail testing mode. In pass/fail testing mode, the BIST 130 tests each location of the RAM 142.1 for defects. If a location of the memory array 142.1 has defective bit(s), the tester 110 is notified via connection 950 as described above related to the read cycle. However, the exact position of the failing bit(s) is not identified. If Diag_Shift = 1 (high), the memory chip 120 is in diagnostic shifting mode in which the content of the failing location is shifted out of the memory chip 120 into the tester 110 via connection 950, and the content of the failing location is also restored back to its original location prior to the shift. As a result, the exact position of the failing bit(s) can be identified, and the data out register 144 of the memory 140 can retain its preconditioning value for the next test cycle (more on this later).

In step 220 of the method 200, the tester 110 initializes the BIST 130 via connection 910. After initialization, the BIST 130 performs a predetermined sequence of cycles including setup, write, and read cycles so that all locations of the memory array 142.1 are tested.

Assume for this example that in order to completely test all locations of the memory array 142.1, the BIST 130 has to perform 3000d cycles with cycles 1d-2000d being setup and write cycles and cycles 2001d-3000d being read cycles. The BIST 130 performs these 3000d cycles sequentially (one cycle at a time) and without pause to completion. This is considered the first testing pass of the testing of the RAM 140.1. The tester 110 will store the failing cycle numbers in tester memory (not shown), for use later.

Assume further for this example that, read cycles 2200d and 2400d are the only two failing cycles identified during the first testing pass. It should be noted that only read cycles can fail. As a result, the tester 110 receives two positive pulses on connection 950 corresponding to cycles 2200d and 2400d.

5 More specifically, during failing read cycle 2200d, the comparator 146.1 pulls connection 948.1 high. With Diag_Shift being low (as a result of step 210), the mode mux 148.1 electrically couples the connection 948.1 to the connections 949.1 and 950. As a result, the connections 949.1 and 950 are also pulled high. With RAM 140.1 being selected for testing (as a result of the scan-in process of step 210), the chip mux 150 electrically couples the connection 950.1 to
10 connection 950. As a result, the connection 950 is also pulled high indicating to the tester 110 that the current cycle (cycle 2200d) is failing. Failing read cycle 2400d has the same effect as failing read cycle 2200d.

In step 230, the tester 110 determines whether there is any failing cycle identified during the first testing pass. Because there are two failing cycles 2200d and 2400d stored in tester
15 memory (not shown), the answer is affirmative. As a result, the method 200 goes to step 240 in which the tester 110 scan-initializes the BIST 130 using the chip's test mode scan chains for a second/final testing pass.

In step 250, the BIST performs the same predetermined sequence of cycles as in the first testing pass described in step 220, except that the BIST 130 stops (pauses) at the next failing cycle which is cycle 2200d. Then, the tester 110 pulls Diag_Shift high to select diagnostic shifting mode. In one embodiment, as a result of Diag_Shift being high, the BIST state register 135 in the BIST 130 and the data-out register 142.1 in the RAM 140.1 become shift registers. Also as a result of Diag_Shift being high, the mode mux 148.1 electrically couples connection 945.1 (coming from data-out register 144.1) to connections 949.1 and 937.1. With RAM select register 136 containing 0b so as to select RAM 140.1 for testing, the BIST mux 137 electrically couples connection 937.1 to connection 937 (leading to the BIST state register 135). As a result, a diagnostic shifting loop is formed comprising (in the shifting direction) the BIST state register 135, connection 935, data-out register 144.1, connection 945.1, connection 949.1, connection 937.1, connection 937, and back to the BIST state register 135. In addition, as a result of Diag_Shift being high, the BIST 130's finite state machine 131 is paused so as to temporarily prevent further test cycles from being invoked.

While the content of the diagnostic shifting loop (i.e., the data-out register 144.1 and the content of the BIST state register 135) is shifted/rotated in the diagnostic shifting loop, the loop content can be extracted out to the tester 110 via connections 950.1 and 950. More specifically, assume that the outputs of the BIST control generator 132, the BIST address generator 133, and the BIST data generator 134 have 2 bits, 15 bits, and 1 bit, respectively, and that the values of these bits are needed for the BIST 130 to resume where it pauses. As a result, the BIST state register 135 need to have 18 bits ($2 + 15 + 1$) for receiving (via connections 932, 933, and 934)

and storing the values of the outputs of the BIST control generator 132, the BIST address generator 133, and the BIST data generator 134, respectively.

Assume further that the memory array 142.1 is 32 bits wide. As a result, the data-out register 144.1 has 32 bits. In one embodiment, in response to Diag_Shift being pulled high by the tester 110, the BIST state register 135 and the data-out register 144.1 shift their contents around the diagnostic shifting loop (clockwise). At the same time, the contents of the data-out register 144.1 and the content of the BIST state register 135 are also extracted to the tester 110 via connection 950.1 and 950. After pulling high Diag_Shift for 50 clocks (32 + 18), the tester 110 pulls Diag_Shift low to switch to pass/fail testing mode. As a result, the BIST state register 135 and the data-out register 144.1 have the same contents as before the shift.

With BIST state register 135 having the same content as before the shift, the BIST 130 can resume from where it pauses. In response to Diag_Shift being pulled low, the BIST resumes where it pauses and moves on to the next cycle (i.e., cycle 2201d).

With the data-out register 144.1 having the same content as before the shift, the testing sequence is not disturbed. More specifically, the pre-conditioning of the content of the data-out register 144.1 such that defect(s) in the next read cycle (if any) can be identified is preserved.

After the shift, in step 260, the tester 110 determines whether there is any next failing cycle identified during the first testing pass (i.e., Step 220) and stored in tester memory. Because there is another failing cycle which is cycle 2400d, the method 200 loops back to step 250. In step 250, the BIST 130 resumes and runs to the next failing cycle which is cycle 2400d and
5 pauses there. Then, the tester 110 pulls Diag_Shift high to select diagnostic shifting mode. In response, the BIST state register 135 and the data-out register 144.1 shift their contents around the diagnostic shifting loop (clockwise). At the same time, the contents of the data-out register 144.1 and the content of the BIST state register 135 are also extracted to the tester 110 via connection 950.1 and 950. After pulling high Diag_Shift for 50 clocks (32 + 18), the tester 110
10 pulls Diag_Shift low to switch to pass/fail testing mode. As a result, the BIST state register 135 and the data-out register 144.1 have the same contents as before the shift.

After the shift, in step 260, the tester 110 determines whether there is any next failing cycle identified during the first testing pass. Because there is no other failing cycle, the method 200 goes to step 270 in which the tester 110 determines whether the RAM being tested (RAM
15 140.1) is the last one. Because there is another RAM to be tested (RAM 140.2), the answer is negative. As a result, the method 200 loops back to step 210.

In step 210, a scan-in of the entire memory chip 120 is performed so that the RAM select register 136 contains 1b (binary) so as to select the RAM 140.2 for testing. Scan-initialization of other circuits (not shown) causes the chip mux 150 to electrically couple the connections 949.2
20 and 950.2 (coming from RAM 140.2) to the connection 950 (coming to the tester 110).

The RAM select register 136 containing 1b causes the BIST mux 137 to electrically couple the connections 937.2 and 949.2 (coming from RAM 140.2) to the connection 937 (leading to the BIST state register 135). As a result, the RAM 140.2 is selected and ready for testing.

5 The testing of the RAM 140.2 is similar to that of the RAM 140.1. More specifically, the diagnostic shifting loop now comprises (in the shifting direction) the BIST state register 135, connection 935, data-out register 144.2, connection 945.2, connection 949.2, connection 937.2, connection 937, and back to the BIST state register 135.

10 Assume further that the memory array 142.2 is 64 bits wide. As a result, the data-out register 144.2 has 64 bits. As a result, the tester 110 needs to shift the diagnostic shifting loop 82 times ($64 + 18$) so as to obtain the contents of the data-out register 144.2 and the BIST state register 135 and so that the data-out register 144.2 and the BIST state register 135 have the same contents as before the shift. Furthermore, at completion of the shift, the BIST 130's finite state machine 131 will resume from the temporarily paused last state before the shift.

15 After the data associated with the last failing cycle is collected, the method 200 goes to step 270 where the tester 110 determines whether the RAM being tested (RAM 140.2) is the last one. Because the RAM 140.2 is the last one to be tested, the answer is affirmative. As a result, the method 200 stops.

With the contents of the failing locations of the RAMs 140.1 and 140.2 collected by the tester 110, analysis can be done to identify the exact positions of the failing bits of these locations.

In FIG. 2, for simplicity, some existing connections are not shown. For instance, the connections 932, 933, and 934 from the BIST control generator 132, the BIST address generator 133, and the BIST data generator 134, respectively, are also connected (but not shown) to the memory array 142.2. The connection 934 from the BIST data generator 134 is also connected (but not shown) to the comparator 146.2 via connection 946.2.

In summary, for each RAM 140.i, the BIST 130 runs only two passes. During the first testing pass, the BIST 130 sequentially and without pause runs through a predetermined sequence of cycles while the tester 110 collects the cycle numbers of the failing cycles.

During the second/last testing pass, the BIST 130 sequentially runs through the same cycles as in the first testing pass, but pauses at each failing cycle identified in the first testing pass so that the tester 110 can collect the content of the location associated with the failing cycle. In the example above, for the RAM 140.1, there are two failing cycles 2200d and 2400d identified during the first testing pass. As a result, during the second testing pass, the BIST 130 pauses a first time for 50 clocks for the tester 110 to collect the content of the location associated with the failing cycle 2200d, and pauses a second time for 50 clocks for the tester 110 to collect the content of the location associated with the failing cycle 2400d. In general, for the RAM 140.1, if M (a positive integer) failing cycles are identified during the first testing pass, then during the second testing pass, the BIST 130 pauses M times for 50 clocks per pause. As a result, a lot of

tester time is saved compared with the case of prior art where the BIST has to restart from cycle 1 (as opposed to resuming) after the content of the location associated with each failing cycle is collected by scanning-out the entire the memory chip.

In the embodiments described above, the memory chip 120 (FIG. 1) has only two RAMs 140.1 and 140.2. In general, the memory chip 120 can have any number of RAMs. For example, assume the memory chip 120 has 2^N RAMS (N is a positive integer). As a result, the RAM select mux 137 needs to have 2^N inputs, the chip mux 150 needs to have 2^N inputs, and the RAM select register 136 needs to have N bits. Alternately, a chip could contain P BISTs 130, whereby not all SRAMs share the same BIST 130, and the number of SRAMs sharing a BIST 130 is less than N, in which case, the BIST multiplexer 137 would need to have less than N inputs. In this case however, the chip mux 150 would still require N inputs (one for each SRAM on the chip).

In the embodiments described above, the BIST state register 135 has 18 bits. In general, the BIST state register 135 can have any number of bits depending on how many bits of the outputs of the BIST control generator 132, the BIST address generator 133, and the BIST data generator 134 need to be saved so that the BIST 130 can resume later.

In the embodiments described above, the RAM 140.1 and 140.2 are 32 bits and 64 bits wide. In general, a RAM 140.i can be K bits wide (K is positive integer). Then, if the BIST state register 135 has L bits (L is positive integer), the associated loop needs to be shifted K + L times at a pause.

While particular embodiments of the present invention have been described herein for purposes of illustration, many modifications and changes will become apparent to those skilled in the art. Accordingly, the appended claims are intended to encompass all such modifications and changes as fall within the true spirit and scope of this invention.